L Number	Hits	Search Text	DB	Time stamp
1	3274	438/624,633,634,637,687.ccls.	USPAT; US-PGPUB	2003/04/28 10:31
2	2121	438/624,633,634,637,687.ccls. and @ad<=20000128	USPAT; US-PGPUB	2003/04/28 10:32
3	1995	(438/624,633,634,637,687.ccls. and @ad<=20000128) and (opening or recess or trench or via or hole)	USPAT; US-PGPUB	2003/04/28 10:32
4	712	((438/624,633,634,637,687.ccls. and @ad<=20000128) and (opening or recess or trench or via or hole)) and copper and barrier	USPAT; US-PGPUB	2003/04/28 10:35
6	414	(((438/624,633,634,637,687.ccls. and @ad<=20000128) and (opening or recess or trench or via or hole)) and copper and barrier) and cmp	USPAT; US-PGPUB	2003/04/28 10:27
9	1725	257/751,760,762.ccls.	USPAT; US-PGPUB	2003/04/28 10:32
10	1213	257/751,760,762.ccls. and @ad<=20000128	USPAT; US-PGPUB	2003/04/28 10:32
11	1043	(257/751,760,762.ccls. and @ad<=20000128) and (opening or recess or trench or via or hole)	USPAT; US-PGPUB	2003/04/28 10:34
12	415	((257/751,760,762.ccls. and @ad<=20000128) and (opening or recess or trench or via or hole)) and copper and barrier	USPAT; US-PGPUB	2003/04/28 10:33
13	383	(((257/751,760,762.ccls. and @ad<=20000128) and (opening or recess or trench or via or hole)) and copper and barrier) not ((((438/624,633,634,637,687.ccls. and @ad<=20000128) and (opening or recess or trench or via or hole)) and copper and barrier) and cmp)	USPAT; US-PGPUB	2003/04/28 10:34
14	1358	sacrificial and semiconductor	EPO; JPO; DERWENT; IBM_TDB	2003/04/28 10:34
15	616	(sacrificial and semiconductor) and (opening or recess or trench or via or hole)	EPO; JPO; DERWENT; IBM_TDB	2003/04/28 10:34

DOCUMENT-IDENTIFIER: US 20010051420 A1

TITLE: Dielectric formation to seal porosity of low dielectic constant (low k) materials after etch

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[0023] As shown in FIG. 1, a first dielectric layer 120 and a first conductive structure 140 (such as a copper intermetal **via** connection) may be formed above a structure 100 such as a semiconducting substrate. However, the present invention is not limited to the formation of a Cu-based interconnect above the surface of a semiconducting substrate such as a silicon wafer, for example. Rather, as will be apparent to one skilled in the art upon a complete reading of the present disclosure, a Cu-based interconnect formed in accordance with the present invention may be formed above previously formed semiconductor devices and/or process layer, e.g., transistors, or other similar structure. In effect, the present invention may be used to form process layers on top of previously formed process layers. The structure 100 may be an underlayer of semiconducting material, such as a silicon substrate or wafer, or, alternatively, may be an underlayer of semiconductor devices (see FIG. 10, for example), such as a layer of metal oxide semiconductor field effect transistors (MOSFETs), and the like, and/or a metal interconnection layer or layers (see FIG. 9, for example) and/or an interlayer dielectric (ILD) layer or layers, and the like.

[0027] As shown in FIG. 2, a metallization pattern is then formed by using the patterned photomask 150, the etch stop layer's 160 and 110 (FIGS. 1-2), and photolithography. For example, openings (such as an opening or trench 220 formed above at least a portion of the first conductive structure 140) for conductive metal lines, contact **holes, via holes,** and the like, are etched into the second dielectric layer 130 (FIG. 2). The opening 220 has sidewalls 230. The opening 220 may be formed by using a variety of known anisotropic etching techniques, such as a reactive ion etching (RIE) process using hydrogen bromide (HBr) and argon (Ar) as the etchant gases, for example. Alternatively, an RIE process with CHF.sub.3 and Ar as the etchant gases may be used, for example. Dry etching may also be used in various illustrative embodiments. The etching may stop at the etch stop layer 110 and at the first conductive structure 140.

[0039] As shown in FIG. 9, the Cu-interconnect layer 800 may be an underlying structure layer (similar to the structure 100) to a Cu-interconnect layer 900. The Cu-interconnect layer 900 may include a Cu-filled trench 940 and an intermetal **via** connection 910 adjacent treated regions 945 of planarized low K dielectric layer 935. The intermetal **via** connection 910 may be a Cu structure similar to the first Cu structure 140, and the intermetal **via** connection 910 may be annealed to the Cu-filled trench 940 in a similar fashion to the anneal described above in relation to the formation of the Cu-interconnect 745 (FIG. 7). The Cu-interconnect layer 900 may also include the etch stop layer 820 and/or etch stop layer 915 and/or etch stop layer 920 (also known as "hard masks" and typically formed of silicon nitride,

Si.sub.3N.sub.4, or SiN, for short) formed and patterned above the planarized low K dielectric layers 925 and/or 935, respectively. The etch stop layer 920 may also be formed above at least a portion of the Cu-filled trench 940.

[0040] As shown in FIG. 10, an MOS transistor 1010 may be an underlying structure layer (similar to the structure 100) to a Cu-interconnect layer 1000. The Cu-interconnect layer 1000 may include Cu-filled trenches 1020 and copper intermetal **via** connections 1030 adjacent treated regions 1050 of a planarized low K dielectric layer 1040. The copper intermetal **via** connections 1030 may be Cu structures similar to the first Cu structure 140, and the copper intermetal **via** connections 1030 may be annealed to the second Cu structures 1020 in a similar fashion to the anneal described above in relation to the formation of the Cu-interconnect 745 (FIG. 7).

[0041] As shown in FIG. 11, a first dielectric layer 1105 and a first conductive structure 1125 (such as a copper intermetal **via** connection) may be formed above a structure 1100 such as a semiconducting substrate. However, the present invention is not limited to the formation of a Cu-based interconnect above the surface of a semiconducting substrate such as a silicon wafer, for example. Rather, as will be apparent to one skilled in the art upon a complete reading of the present disclosure, a Cu-based interconnect formed in accordance with the present invention may be formed above previously formed semiconductor devices and/or process layer, e.g., transistors, or other similar structure. In effect, the present invention may be used to form process layers on top of previously formed process layers. The structure 1100 may be an underlayer of

semiconducting material, such as a silicon substrate or wafer, or, alternatively, may be an underlayer of semiconductor devices (see FIG. 20, for example), such as a layer of metal oxide semiconductor field effect transistors (MOSFETs), and the like, and/or a metal interconnection layer or layers (see FIG. 19, for example) and/or an interlayer dielectric (ILD) layer or layers, and the like.

[0043] As will be described in more detail below in conjunction with FIG. 12, the first etch stop layer 1110 and a second etch stop layer 1115 define a lower (**via**) portion of the copper interconnect formed in the dual-damascene copper process flow. If necessary, the third dielectric layer 1130 may be planarized using chemical-mechanical planarization (CMP). The third dielectric layer 1130 has an etch stop layer 1160 (typically also SiN) formed and patterned thereon, between the third dielectric layer 1130 and the patterned photomask 1150.

[0046] As shown in FIG. 12, a metallization pattern is then formed by using the patterned photomask 1150, the etch stop layer's 1160, 1115 and 1110 (FIGS. 11-12), and photolithography. For example, first and second **openings, such as via** 1220 and trench 1230, for conductive metal lines, contact **holes, via holes,** and the like, are etched into the second and third dielectric layers 1120 and 1130, respectively (FIG. 12). The first and second openings 1220 and 1230 have sidewalls 1225 and 1235, respectively. The first and second openings 1220 and 1230 may be formed by using a variety of known anisotropic etching techniques, such as a reactive ion etching (RIE) process using hydrogen bromide (HBr) and argon (Ar) as the etchant gases, for example.

Alternatively, an RIE process with CHF.sub.3 and Ar as the etchant gases may be used, for example. Dry etching may also be used in various illustrative embodiments. The etching may stop at the etch stop layer 1110 and at the first conductive structure 1125.

[0055] As shown in FIG. 16, this process typically produces a conformal coating of Cu 1640 (or another conductive material) of substantially constant thickness across the entire conductive surface 1535. As shown in FIG. 17, once a sufficiently thick layer of Cu 1640 has been deposited, the layer of Cu 1640 is planarized using chemical mechanical polishing (CMP) techniques. The planarization using CMP clears all Cu and barrier metal from the entire upper surface 1530 of the third dielectric layer 1130, leaving the Cu 1640 only in a metal structure such as a Cu-filled **trench and via,** forming a Cu-interconnect 1745, adjacent remaining portions 1725A and 1725B of the one or more barrier metal layers 1525A and copper seed layer 1525B (FIGS. 15 and 16), respectively, as shown in FIG. 17.

[0058] As shown in FIG. 19, the Cu-interconnect layer 1800 may be an underlying structure layer (similar to the structure 1100) to a Cu-interconnect layer 1900. In various illustrative embodiments, the Cu-interconnect layer 1900 may include a Cu-filled trench 1940 adjacent treated regions 1945 of a planarized low K dielectric layer 1935, an intermetal **via** connection 1910 adjacent a planarized low K dielectric layer 1925, and an etch stop layer 1915 between the low K dielectric layers 1935 and 1925. The intermetal **via** connection 1910 may be a Cu structure similar to the first Cu structure 1125, and the intermetal **via** connection 1910 may be annealed to

the Cu-filled trench 1940 in a similar fashion to the anneal described above in relation to the formation of the Cu-interconnect 745 (FIG. 7). The Cu-interconnect layer 1900 may also include the etch stop layer 1820 and/or an etch stop layer 1920 formed and patterned above the planarized low K dielectric layer 1935 and above at least a portion of the Cu-filled trench 1940.

[0061] The dual-damascene copper process flow according to various embodiments of the present invention, as shown in FIGS. 11-18, combines the intermetal **via** connection formation with the Cu trench-fill formation by etching a more complex pattern before the formation of the barrier metal layer and Cu seed layer and before the Cu trench-fill. The trench etching continues until the **via hole** (such as the first opening 1220 in FIG. 12) has been etched out. The rest of the dual-damascene copper process flow according to various embodiments of the present invention, as shown in FIGS. 13-18, is essentially identical with the corresponding single-damascene copper process flow according to various embodiments of the present invention, as shown in FIGS. 3-8. Overall, however, the dual-damascene copper process flow according to various embodiments of the present invention significantly reduces the number of processing steps and is a preferred method of achieving Cu-metallization.

21. A method of forming a copper interconnect, the method comprising: forming a first dielectric layer above a structure layer; forming a first opening in the first dielectric layer; forming a **copper via** in the first opening; forming a second dielectric layer above the first dielectric layer and above the **copper via**; forming a second opening in the

second dielectric layer above at least a portion of the **copper via,** the second opening having sidewalls having open pores; and forming a third dielectric layer on the sidewalls of the second opening to cover the open pores.

22. The method of claim 21, further comprising: forming a copper line in the second opening, the copper line contacting the at least the portion of the **copper via**; and forming the copper interconnect by annealing the copper line and the **copper via**.

31. A method of forming a copper interconnect, the method comprising: forming a first dielectric layer above a structure layer; forming a first opening in the first dielectric layer; forming a first copper layer above the first dielectric layer and in the first opening; forming a **copper via** by removing portions of the first copper layer above the first dielectric layer, leaving the **copper via** in the first opening; forming a second dielectric layer above the first dielectric layer and above the **copper via**; forming a second opening in the second dielectric layer above at least a portion of the **copper via,** the second opening having sidewalls having open pores; and forming a third dielectric layer on the sidewalls of the second opening to cover the open pores.

32. The method of claim 31, further comprising: forming a second copper layer above the second dielectric layer and in the second opening, the second copper layer contacting the at least the portion of the **copper via**; forming the copper interconnect by removing portions of the second copper layer above the second dielectric layer, leaving the copper interconnect in the second

opening; and annealing the copper interconnect.